EXHIBIT C

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Title: FAILSAFE PRINCIPLE: A FAILING CLOCK SOURCE IN AN ASYNCHRONOU

Search criteria:

An International Novelty Search was conducted in respect of an asynchronous method for handling a failing clock in an electronic system. A clock source is used that has a status output that shows the status if the oscillator is running. This output is connected to an interrupt request of the microcontroller, which can then detect an error condition. This will start a software routine that handles code related to a failing clock source without the need of the clock source

Very Relevant Documents (* indicates a Philips patent/application)	relevant to criteria

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Technical Background (* indicates a Philips patent/application)	relevant to criteria

EP385404 (1) abstract
US 5226152 (2) abstract
US 5291528 (3) abstract
US 5946362 (4) abstract
US 6343334 (5) abstract

1. Clock failure recovery in a processing system.

2. Watchdog timer for detecting an error condition for non-responding processors.

3. Glitch-free switching of asynchronous clock sources.

4. Clock failure detection in a synchronous system by measuring intervals between clock pulses.

5. Use of a watchdog timer to detect the stopping of a clock oscillation